Wafer Level Fan-Out (WLFO)

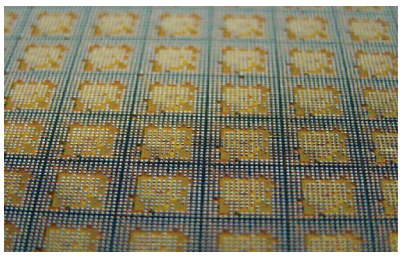
Wafer level packaging applies similar processes as used in front-end wafer processing. One advantage is batch processing, where all components on a large wafer format are efficiently processed simultaneously.

Today's trend is "More than Moore", and involves heterogeneous integration of different elements in package level and embedded technologies. Reducing the form factor while increasing the number of I/Os is necessary to integrate more functionality in the system. Fan-Out WLP is the answer to those challenges. This allows system integration at the wafer-level with the highest integration density.

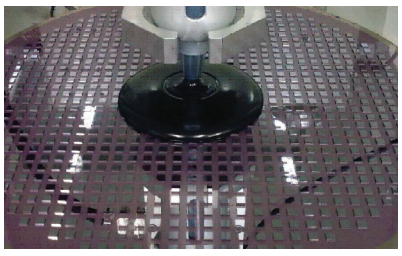
Amkor is licensed to use fan-out WLP technology eWLB (embedded Wafer Level Ball Grid Array) and is one of the leading drivers of this new packaging technology platform. Together with its partner, Amkor developed the 300 mm reconstituted wafer solution, ramping this technology into high volume manufacturing. As of today, over 2 billion eWLB components have been shipped.

Design Features

- Chip-first approach with Known Good Die (KGD) from probed front-end wafers
- Supports all kinds of incoming wafer diameter and chip packaging media
- Reconstituted wafer (chip embedding in epoxy)
- Single die and multi-die solutions, possibility of embedded discrete passives
- Package size: from below 1 x 1 mm² to 12 x 12 mm² (up to 25 x 25 mm² under development)
- Package thickness: 0.3-1.0 mm
- Single-layer RDL/dual-layer RDL
- Double-sided RDL for Package-on-Package (PoP) applications under development
- Several UBM types for improved reliability
- BGA bump pitch down to 0.400 mm (down to 0.300 mm under development)
- Bare die backside for heat spreader assembly, overmold or backside coating by tape
- Standard laser marking and packing



Bumped wafer



Dispensed mold compound

Amkor Technology®

WLFO

Applications

- Mobile and consumer products, baseband, RF, analog, power management
- ASIC, MEMS, system solutions for medical, security, encryption, DC/DC converter, radar and automotive
- Electro-Optical WLSiP, solutions for M2M communication and Internet of Things (IoT)
- Extension of the technology platform to a wider field of application areas is ongoing

Differentiation

- Chip size independent package design with small package size adder
- High degree of package design freedom, fan-out zone adaptable to customer needs
- No restrictions in bump pitch, covering I/O gap between IC and PCB
- No laminate substrate required, shorter interconnections, excellent electrical performance
- Lower thermal resistance compared to Flip Chip in Package (FCiP) and conventional substrate based BGA
- System-in-Package on Wafer-Level (WLSiP) and Package-on-Package (PoP) solutions
- Smaller footprint and thinner package than FCiP BGA, no need for underfill
- Reliable, miniaturized high performance package
- RoHS and REACH compliant package
- Cost effective due to 300 mm wafer batch processing and no need of extra interposer
- Highly simplified supply chain and manufacturing infrastructure
- Better board level reliability and backside protection compared to WLCSP

Thermal

Strongly dependent on chip size to package size ratio, RDL line width and thickness, number and position of I/Os, type of backside protection. Example for reference: Package size 8 x 8 mm, chip size 5 x 5 mm shows thermal performance Rth junction-ambient = 32.5 K/W and Rth junction-case = 6.5 K/W.

Electrical

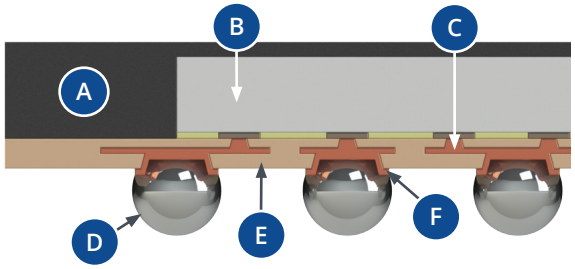
Excellent performance data compared to conventional wirebonded BGA and FCiP with significantly reduced package parasitics.

Interconnect Level	BGA	FCiP	eWLB
Resistance @ DC [mO]	76	7.5	3.2
Resistance @ 5 GHz [mO]	375	41	15
Inductance [nH]	1.100	0.052	0.018

Package Level	BGA	FCiP	eWLB
Resistance @ DC [mO]	89	22	23
Resistance @ 5 GHz [mO]	629	248	91
Inductance [nH]	1.790	0.950	0.340

Due to the very low inductance values, this package type is excellent for high speed applications, such as RF and radar, proven up to 81 GHz.

Cross Section



- A Fan-out area (mold)
- B Chip
- C Redistribution Layer (RDL)
- D Solder Ball
- E Dielectric
- F UBM (in CSP^{nl})

WLFO

Performance Data: Reliability

Component Level Tests

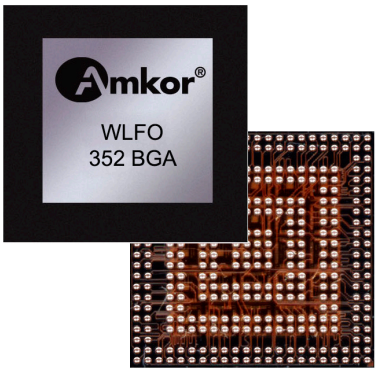
(9.25 x 8.80 mm², single die, 1L-Cu-RDL, no UBM, 222 bumps, 0.400 mm pitch)

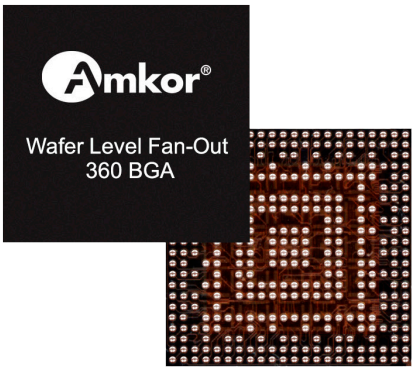
Test	Specification	Criteria
Moisture Sensitivity Level (MSL)	IPC/JEDEC J-STD-020	MSL1 For Lead-Free, 168 Hours At 85°C/85% RH
Temperature Cycling (TC)	JESD22-A104, Condition B	-55°C/125°C, 2 Cy/Hour, 1000 Cycles
High Temperature Storage (HTS)	JESD22-A103, Condition B	150°C, 2000 Hours
Unbiased HAST (uHAST)	JESD22-A118, Condition A	130°C/85% RH, 96 Hours

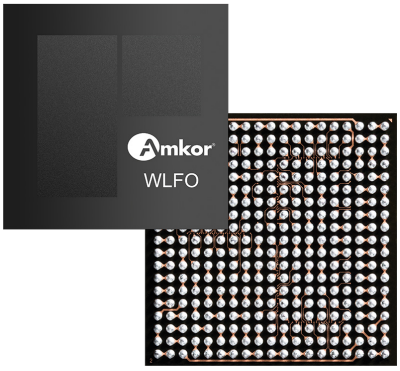
Board Level Tests

(9.25 x 8.80 mm², single die, 1L-Cu-RDL, no UBM, 222 bumps, 0.400 mm pitch)

Test	Specification	Criteria
Temperature Cycling on Board (TCoB)	IPC-97-01	-40°C/125°C, 1 Cy/Hour, 1000x
Drop Test	JESD22-B111	30 Drops







WLCSP+

Overview

Amkor has applied its WLFO technology know-how, taking Wafer Level CSP (WLCSP) to the next packaging generation: WLCSP+.

- Recon wafer is created with KGD (Known Good Die) placed with very small distance between dies
- All solder balls are placed in the fan-in zone
- Mold compound offers 5-side mechanical die protection (sidewalls and optional backside protection)
- Compared to WLCSP, WLCSP+ offers an additional 50% increase in die strength
- Diced die test on wafer-level without bare die handling
- Components can be delivered in JEDEC tray without risk
- WLCSP manufacturing in highly efficient 300 mm WLFO recon wafer, independent of wafer diameter provided by the customer

Design Features

- Supports 300 mm wafer diameter
- Single/multi-layer Cu RDL, with and without Cu UBM
- Max package size: 23 x 25 mm^2 (largest in the market)
- Min package thickness: 0.4 mm (thinner under validation)
- Plated RDL line/space width: 20/20 µm (10/10 µm under validation)
- Bump height and pitch: 0.25 mm @ 0.5 mm (down to 0.2 mm @ 0.4 mm under validation)
- Backside coating optional
- Standard laser marking and packing in tape and reel

Applications

- Mobile and consumer products, handsets
- Wireless connectivity including Bluetooth, WLAN, RF, FM radio, GPS
- PMIC, PMU, high performance computing
- Analog and other ICs such as MEMS and Sensors

Performance

- **Electrical:** Low parasitics due to short connections (WLCSP), thick Cu- RDL and choice of dielectric material (LTC-PI). Dependent on design and application suitable for 10 GHz and beyond
- **Thermal:** Depending on die size and whether backside die is molded/exposed (e.g., 5 x 5 mm^2 die, molded backside die: Rth = 30 K/W)

Performance Data: Reliability

6.6 x 7.1 x 0.4 mm^3, 98 bumps, 500 µm pitch; WLCSP+ with 30 µm sidewall + backside mold. Stack-up: PBO/Cu RDL/PBO/Cu UBM.

Component Level Tests

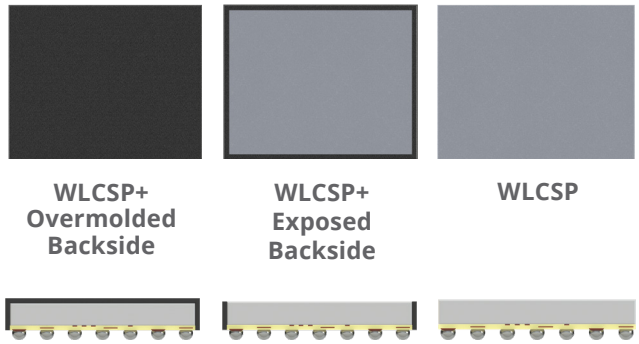
Test	Specification	Criteria
Moisture Sensitivity Level (MSL)	IPC/JEDEC J-STD-020	MSL1 For Lead-free, 168 Hrs at 85°C/85% RH
Temperature Cycling (TC)	JESD22-A104, Condition B	-55°C/125°C, 2 Cy/Hour, 1000 Cycles
High Temperature Storage (HTS)	JESD22-A103, Condition B	150°C, 2000 Hours
Unbiased HAST (uHAST)	JESD22-A118, Condition A	130°C/85% RH, 96 Hours

Board Level Tests

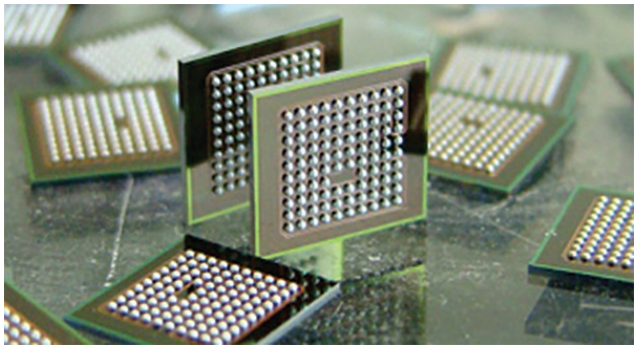
Test	Specification	Criteria
Drop Test	JESD22-B111	30 Drops
Temperature Cycling on Board (TCoB)	IPC-97-01	-40°C/125°C, 1 Cy/Hour, 1000x

WLCSP+

Backside and Cross Sections



Singulated Components



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